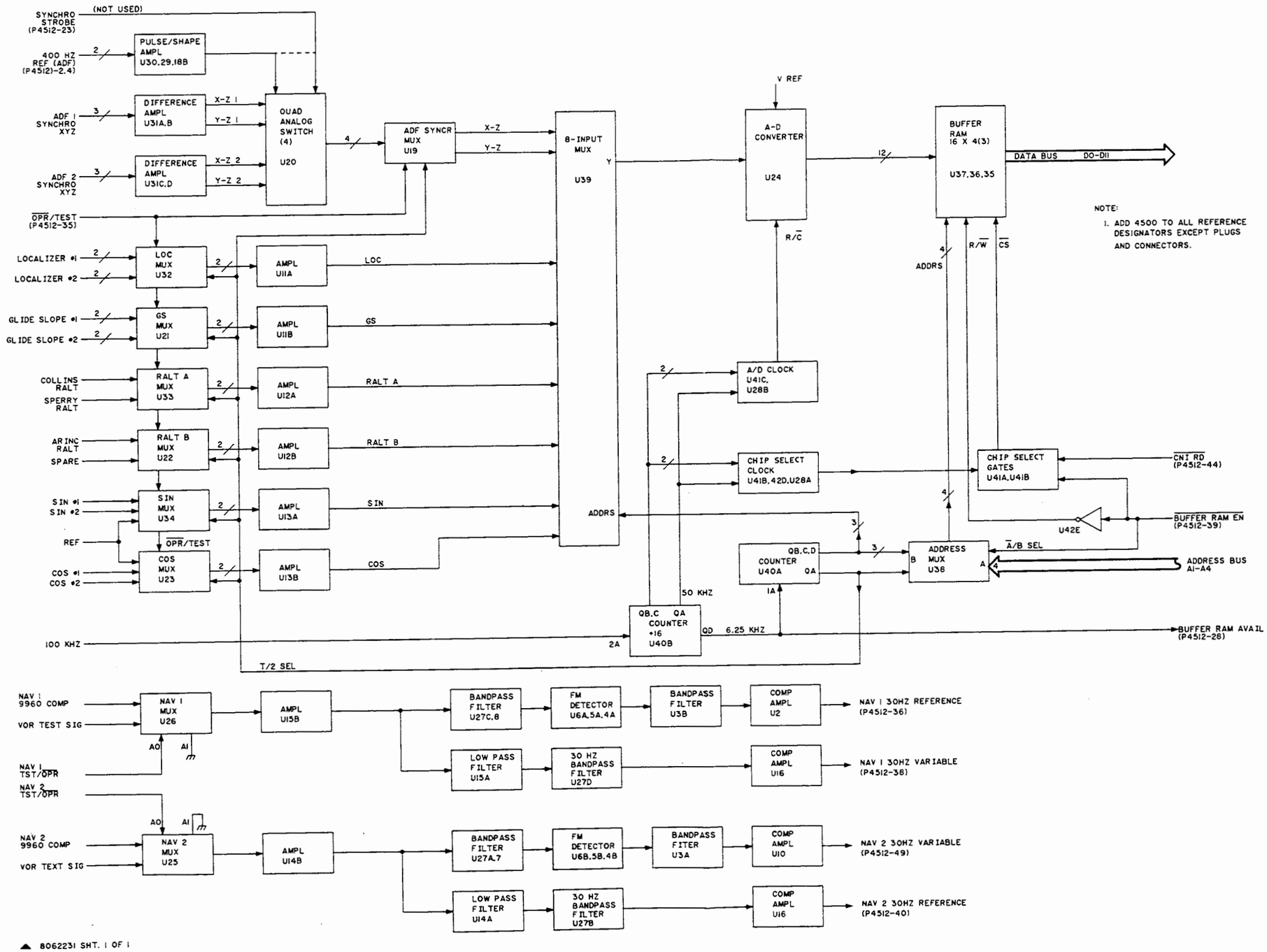


CNI Analog Module, Simplified Block Diagram
Figure 78

(8) CNI Analog Modules, 3605609-0501, -0503, and -0550

(a) General (See figure 78)

Three different CNI analog modules are currently installed in the NC-104B, depending upon the functions required. The 3605609-0501 part number module is described in the following paragraphs. The -0503 module contains only the RALT circuits, which are identical on all modules. The -0550 is similar to the -0501, -0503 module except for HIRF lightning protection circuitry.

This module processes the analog CNI signals from non-ARINC 429 equipment, and generates digital signals for incorporating into an ARINC 429 word.

This paragraph and the following paragraph 7.C(9) describe the CNI interface circuits. Although this module processes the analog inputs, and the following CNI digital module processes the digital inputs, the two modules have some common areas. Refer to the block diagram description for an overall description of the CNI interface circuits.

The CNI analog module receives DC level inputs from the GS/LOC portion of the NAV receiver, analog inputs from the radio altimeter, and the sin/cos or synchro converter inputs fed by the ADF receiver.

The 9960 Hz VOR bearing composite signal from the NAV receiver is also applied to this module for processing.

An interface is provided for both left and right side inputs, except for the radio altitude (RALT) data input. Figure 79 lists the inputs processed by the CNI analog module.

INPUT SIGNALS	MULTIPLEXER EMPLOYED
ADF 1 SYNCHRO X, Y, Z	U4519
ADF 2 SYNCHRO X, Y, Z	U4519
ADF SIN 1	U4534
ADF SIN 2	U4534
ADF COS 1	U4523
ADF COS 2	U4523
Localizer 1	U4532
Localizer 2	U4532

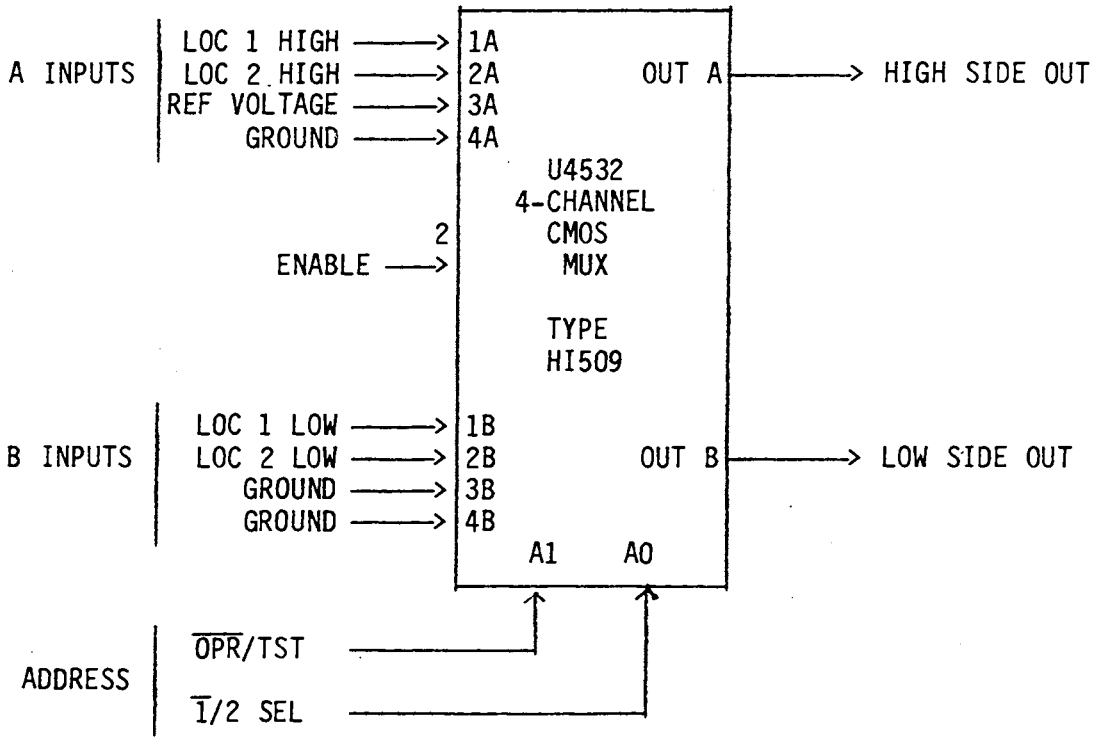
INPUT SIGNALS	MULTIPLEXER EMPLOYED
Glideslope 1	U4521
Glideslope 2	U4521
Collins RALT	U4533
Sperry RALT	U4533
ARINC RALT	U4522
NAV 1 9960 composite	U4526
NAV 2 9960 Composite	U4525
VOR test	U4525, U4526

Input Signals and Multiplexers Employed
Figure 79

(b) Input Multiplexers

Several 4-channel CMOS analog multiplexers (type HI509) are contained on the module, and are used for selecting inputs to be processed. Refer to figure 79 and 80.

This chip has four "A" inputs and four "B" inputs, with a single "A" output and a single "B" output. When the chip is enabled by a logic high at pin 2, one of the "A" inputs will appear at the "A" output, and one of the "B" inputs will appear at the "B" output. A 2-bit address (A1, A0) determines which of the four inputs is switched to the output. All the multiplexers (except the two NAV mux's) are addressed simultaneously by the $\overline{I}$/2 SEL signal and the $\overline{OPR}$/TST signal.



Typical Analog Multiplexer Operation
Figure 80

(c) ADF Synchro Inputs

The ADF synchro supplies three signals (X, Y, and Z) of varying phase. Two ADF synchro inputs can be processed.

The ADF 1 synchro X and Z inputs are applied to difference amplifier U4531B which produces an X-Z output. The Y and Z inputs are applied to difference amplifier U4531A which produces a Y-Z output. The two outputs are applied to analog switch U4520.

Similarly, the ADF 2 inputs are subtracted and the resulting signals are applied to analog switch U4520. This chip is a quad SPST analog switch. Each of the four switches in the chip can be operated independently by an "A" input, however, in this circuit all are operated by an output from multivibrator U4518B, which is triggered by the 400 Hz reference input that operates the synchros. The switch gates the four ADF signals to ADF multiplexer U4519.

The ADF multiplexer selects the ADF 1 or the ADF 2 inputs, or a reference voltage input, depending upon the address. Refer to figure 81 for ADF multiplexer addresses. The selected signals are applied to 8-input multiplexer U4539, for application to the analog-to-digital (A/D) converter (U4524).

ADDRESS		SELECTED SIGNALS
$\overline{OPR}$/TST	$\overline{I}$/2 SEL	
0	0	ADF 1 synchro, X-Z and Y-Z
0	1	ADF 2 synchro, X-Z and Y-Z
1	0	Reference voltage test
1	1	Circuit off, set test

ADF Synchro Multiplexer U4519 Addresses
Figure 81

(d) Localizer Inputs

The two localizer inputs are applied to multiplexer U4532. Either the high and low LOC 1 inputs are selected or the high and low LOC 2 inputs are selected. The addresses are the same as previously shown for the ADF synchro multiplexer (mux) in figure 81. The selected inputs are applied to integrating amplifier U4511A, which supplies the selected LOC signal to 8-input multiplexer U4539.

(e) Glideslope Inputs

The two glideslope (GS) inputs are processed by multiplexer U4521, exactly like the LOC signals. The selected GS signal is also applied to multiplexer U4539.

(f) RALT Multiplexers

Two multiplexers (U4533 and U4522) are provided for selecting up to four RALT inputs. Currently only three of the four possible inputs are employed. Multiplexer U4533 (RALT A) is wired to receive a Collins RALT or a Sperry RALT. Multiplexer U4522 is wired to receive an ARINC RALT and a spare RALT input. The inputs are processed exactly like the LOC and GS inputs, and the RALT A and RALT B inputs are applied to multiplexer U4539.

(g) Sine and Cosine Multiplexers

These two multiplexers (U4534 and U4523) receive the sine (SIN) and cosine (COS) signals respectively from two ADF units. The analog signals are processed exactly like the previously described multiplexers. The SIN output from U4534 and the COS output from U4523 are also applied to multiplexer U4539.

(h) Eight-Input Multiplexer U4539

This chip selects one of eight inputs for application to the analog-to-digital converter U4524. The input that is selected is determined by the 4-bit address from dual counter U4540A. The least significant bit (U4540-3) is the $\overline{1}/2$ SEL bit and the other three bits directly address the multiplexer. Figure 82 lists the address scheme for the multiplexer, and illustrates how the inputs are sequentially sampled. The operate mode is assumed (the $\overline{OPR}$/TST signal is low).

As previously described, all of the input multiplexers are continuously enabled, and are all addressed by the same 2-bit address. Therefore, the eight input circuits will all be supplying output data, depending upon the address. That necessitates the 8-input multiplexer to select one of the inputs at a time for application to the A/D converter.

U4539 ADDRESS				INPUT SELECTED	RAM ADDRESS	U4539 ADDRESS				INPUT SELECTED	RAM ADDRESS
A2	A1	A0	$\overline{I}/2$			A2	A1	A0	$\overline{I}/2$		
0	0	0	0	ADF X-Z #1	0	1	0	0	0	RALT A #1	8
0	0	0	1	ADF X-Z #2	1	1	0	0	1	RALT A #2	9
0	0	1	0	ADF Y-Z #1	2	1	0	1	0	RALT B #1	10
0	0	1	1	ADF Y-Z #2	3	1	0	1	1	RALT B #2	11
0	1	0	0	LOC #1	4	1	1	0	0	SIN #1	12
0	1	0	1	LOC #2	5	1	1	0	1	SIN #2	13
0	1	1	0	GS #1	6	1	1	1	0	COS #1	14
0	1	1	1	GS #2	7	1	1	1	1	COS #2	15

Multiplexer U4539 and RAM Write Addresses (from U4540A)
Figure 82

(i) Analog-to-Digital Converter U4524

This chip digitizes the dc input voltage (supplied by U4539) into a 12-bit parallel digital word. The chip compares the input voltage with a reference voltage to determine the value, and generates the 12-bit word.

The A/D converter is controlled by three external inputs; CE at pin 6, $\overline{CS}$ at pin 3, and R/$\overline{C}$ at pin 5. In this application, the chip select ($\overline{CS}$) is wired low for permanent selection, the chip enable (CE) is wired to +5 V for permanent enable, and the read/convert (R/$\overline{C}$) input is controlled by flip-flop U4528B. When the $\overline{R}$/C input goes low (400 nsec minimum), the conversion cycle (convert start) is initiated. The actual conversion will start in about 500 nsec, and once the cycle is started, it cannot be interrupted. The conversion cycle requires about 30 usec and then valid data is available. The data will appear at the outputs when the $\overline{R}$/C signal goes high.

When R/$\overline{C}$ is high (after conversion) the data output lines are enabled and the 12-bit word is applied to the buffer RAM, since the 12/$\overline{8}$ format input at pin 2 of the A/D converter is wired high to select a 12-bit word output. The buffer RAM is formed by U4535, U4536, and U4537. Each chip in the RAM provides 16 bits of storage for each of four inputs, therefore, the entire RAM can store 16 12-bit words.

(j) Address and A/D Converter Control Circuits

The multiplexers and A/D converter are addressed by signals generated from a 100 KHz clock input. The clock is applied to a 4-stage counter (U4540B) which divides the 100 kHz by 2, 4, 8, and 16, resulting in outputs of 50 kHz, 25 kHz, 12.5 kHz, and 6.25 kHz respectively. The 6.25 kHz output clocks the second counter (U4540A) and generates four more outputs that are used for the $\overline{1}$/2 SEL signal and the 8-input multiplexer (U4539) address inputs as previously explained.

Refer to timing diagram figure 83. The 50 kHz output at pin 11 clocks D-type flip-flops U4528B and U4528A. The D-input to these F-F is obtained from NORing the 25 kHz and the 12.5 kHz outputs. The $\overline{Q}$ output from U4528B is the R/$\overline{C}$ signal to the A/D converter, and the Q output from U4528A is used for the read signal to the buffer RAM.

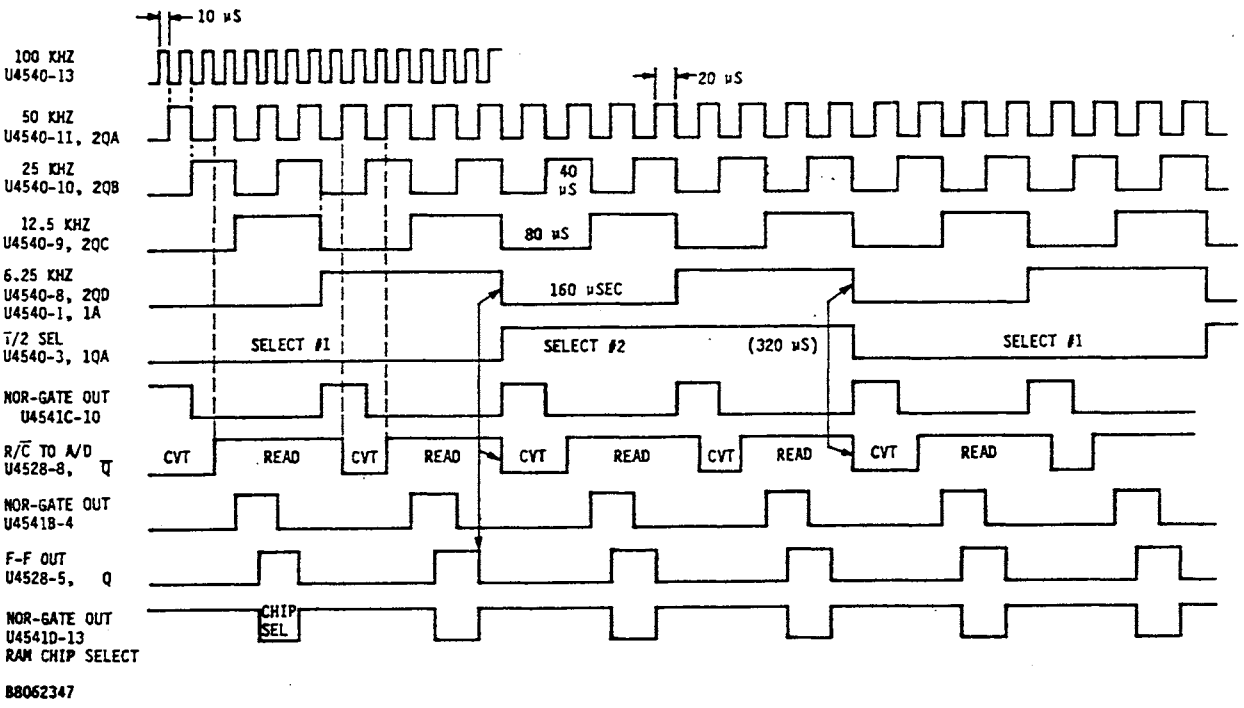
(k) Buffer RAM (U4535-U4537)

The three 64-bit chips in the Buffer RAM are wired to operate as a single RAM, with common read/write, chip select, and address inputs. The total RAM has 12 inputs and can store 16 words. Figure 84 is a timing diagram for the RAM address generated by the counter in U4524A and selected by multiplexer U4538.

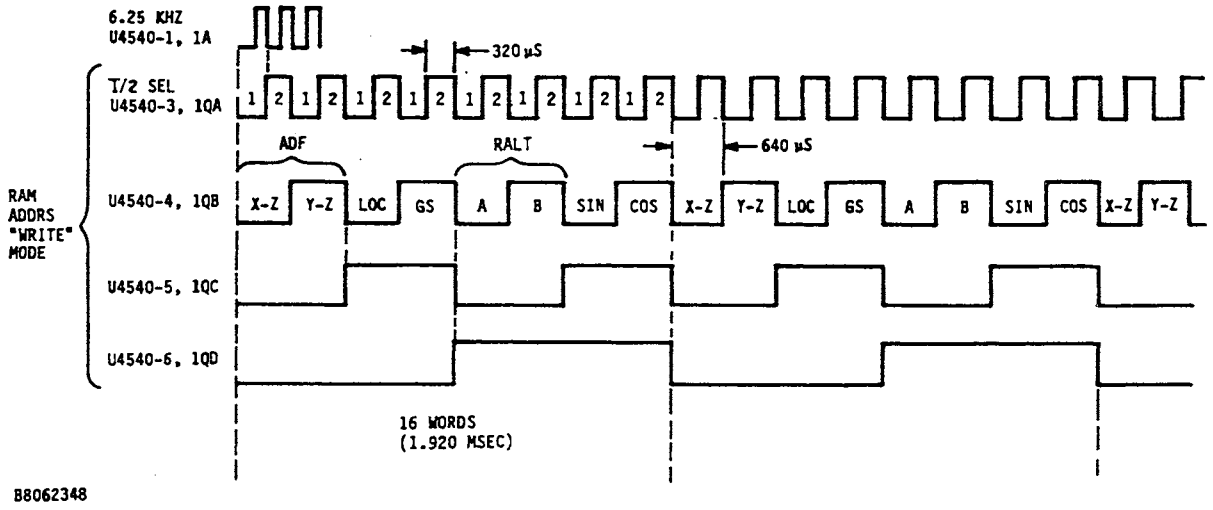
The diagram illustrates the sequential storage of the 16 possible data inputs from the input multiplexers. Once again, observe that while 8-bit multiplexer U4539 is addressed for each of the 8 inputs, the $\overline{1}$/2 SEL bit toggles every 320 microseconds (50 kHz) and applies the #1 and then the #2 input for that addressed selection, creating 16 inputs which are processed by the A/D converter and ultimately supplied to the buffer RAM as 16 12-bit words.

Each 64-bit RAM has an active-low write input ($\overline{WE}$) that controls the writing/reading operation for the memory, and an active-low chip select ($\overline{CS}$) at pin 2. When the $\overline{CS}$ and $\overline{WE}$ are both low, the data on the four inputs (D1 - D4) is written into the addressed memory word, and preconditions the output circuitry so that correct data is present at the outputs when the write cycle is complete.

Reading is performed when the chip select is low and the write input is high. The data stored in the addressed word is read out on the four non-inverting outputs. When the chip select (pin 2) is high, and during a writing operation, the four outputs go to an inactive high impedance state.



Analog Mux and A/D Converter Control Timing Diagram
Figure 83



Buffer RAM "Write" Address Timing Diagram
Figure 84

(l) Buffer RAM Address Multiplexer U4538

This chip is a quad 2-input multiplexer with an $\overline{A}$/B select input at pin 1. The chip is permanently enabled by the low input at pin 15. When the select input (pin 1) is low, the four address inputs (A1, A2, A3, A4) from the microprocessor address bus are applied to the multiplexer output pins and address the buffer RAM. When the select input is high, the four B address inputs from counter U4540B are applied to the output pins and address the buffer RAM.

The select input to the multiplexer is the $\overline{\text{BUFFER RAM EN}}$ signal from the CNI digital board. This input (P4512-39) is actually a RAM read enable, and is low when the microprocessor wants to read the analog CNI data from the buffer RAM. At this time the microprocessor will supply the necessary 16 addresses to read the 16 12-bit words in the RAM and the data will be applied to the data bus, in sequence as illustrated in figure 1xx. Observe that the inverted $\overline{\text{BUFFER RAM EN}}$ signal is also the read/write signal to the RAM (pin 3), and results in the "write" mode when the signal is high, as previously explained.

(m) RAM Operation Sequence Summary

1 Write Mode

As previously described, when the $\overline{\text{BUFFER RAM EN}}$ signal is high, the RAM is in the write mode and the 16 dc voltage inputs are continuously being supplied to the A/D converter, converted into a 12-bit digital word, and stored in the buffer RAM without control from the microprocessor. When the microprocessor accesses the buffer RAM to read the accumulated data, the free-running process is halted. However, the control circuits will not permit the processor to interrupt a "write" sequence in the RAM.

2 Read Mode

When the write sequence is complete, the 2QD output from counter U4540B (pin 8) goes low and clocks counter U4540A to select the next multiplexer (U4539) input and advance the write address to the RAM for the next A/D conversion and RAM write cycle. This output from pin 8 of U4540 is also the $\overline{\text{BUFFER RAM AVAIL}}$ signal which is applied to the CNI digital board, where it results in a low $\overline{\text{BUFFER RAM EN}}$ signal and an input to the microprocessor via the data bus.

The low $\overline{\text{BUFFER RAM EN}}$ signal now selects the microprocessor address inputs to U4538. The signal is also inverted by U4542E, which selects the "read" mode for the RAM and clears the counter (U4540B) which generates the clocks for the A/D converter.

The data in the RAM is now read out at a 20 Hz rate, controlled by the microprocessor address from multiplexer U4538. The RAM read address is shown in figure 85.

ADDRESS				READ FUNCTIONS
A4	A3	A2	A1	
0	0	0	0	#1 ADF SYNC X-Z
0	0	0	1	#2 ADF SYNC X-Z
0	0	1	0	#1 ADF SYNC Y-Z
0	0	1	1	#2 ADF SYNC Y-Z
0	1	0	0	#1 LOC
0	1	0	1	#2 LOC
0	1	1	0	#1 GS
0	1	1	1	#2 GS
1	0	0	0	RALT A (Collins)
1	0	0	1	RALT B (Sperry)
1	0	1	0	RALT C (ARINC 552)
1	0	1	1	RALT C offset test
1	1	0	0	#1 ADF sin
1	1	0	1	#2 ADF sin
1	1	1	0	#1 ADF cos
1	1	1	1	#2 ADF cos

Buffer RAM Read Addresses from U4538
Figure 85

(n) NAV Composite Input Circuits

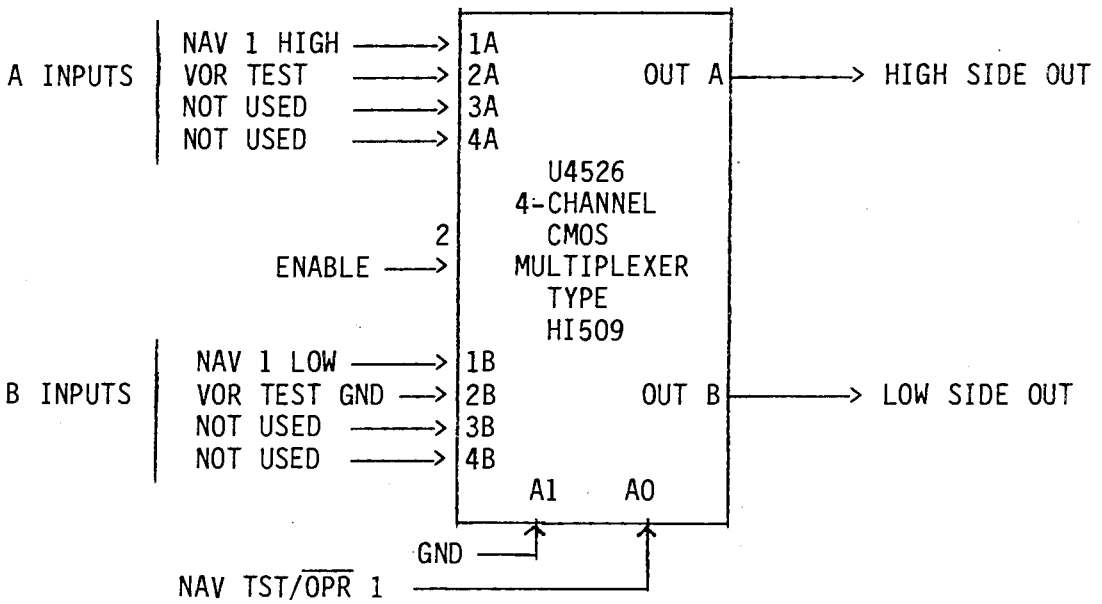
1 General

At this time, recall that the VOR composite signal contains two 30 Hz signals. A reference signal and a variable signal. The two are in-phase only at 0° magnetic North. At all other headings, the phase between the two 30 Hz signals will vary. This results in the familiar composite signal format, with the 9960 Hz signal being frequency modulated by the reference signal and amplitude modulated by the variable phase signal.

There are two identical NAV composite circuits on the board. Each of the NAV composite circuits (VOR decoder) contains three main parts; an input multiplexer, a reference signal decoder, and a variable signal decoder. Only the NAV 1 circuit is described in the following paragraphs.

2 Input Multiplexer U4526

Figure 86 illustrates the input analog multiplexer (U4526) employed for the NAV 1 input. This multiplexer selects either the composite VOR signal from the NAV 1 receiver, or the VOR test signal from the CNI digital board. Only two of the four possible inputs to the multiplexer are used. Therefore, the A1 address input is permanently grounded and only the A0 input (TST/$\overline{\text{OPR}}$) is used to select one of the two input signals.



NAV Composite Multiplexer U4526
Figure 86

When the VOR TST/$\overline{OPR}$ signal is low, the NAV 1 composite input is selected, and when the NAV TST/$\overline{OPR}$ signal is high, the composite VOR test signal is selected. The selected input is applied to a difference amplifier (U4515B), and the resulting composite signal is applied to a "reference" signal decoder and to a "variable" signal decoder.

3 Variable Signal Decoder Circuit

The variable signal decoder circuit contains a low-pass filter (U4515A), a band-pass filter (U4527D) and an output comparator/amplifier (U4517).

The composite Nav signal is coupled by R110 to the low-pass filter. The 30 Hz low-pass filter extracts the 30 Hz variable signal from the composite signal, removing the 9960 Hz signal. The band-pass filter, U4527D, further attenuates the 9960 Hz component.

The filtered 30 Hz signal is then applied to comparator circuit U4517 which converts the sinusoidal waveform into a TTL level (10 V p-p) squarewave signal corresponding to the 30 Hz variable signal. The output at U4517, pin 7 is fed via J4512 pin 38 to the CNI digital module.

4 Reference Signal Decoder Circuit

The purpose of this circuit is to remove the 30 Hz reference signal which frequency modulates the 9960 Hz component of the rf carrier. Refer to figure 87.

This decoder circuit contains a 9960 Hz band-pass filter (U4527C, U4508), an FM detector and pulse averaging circuit (U4506A, U4505A, U4504A), a 30 Hz band-pass filter (U4503B), and a difference/comparator amplifier (U4502).

The 9960 Hz band-pass filter removes the 30 Hz variable frequency component from the VOR signal, resulting in a 9960 Hz FM output signal at pin 8 of U4527C. U4508 is a comparator which converts the sinewave to a squarewave.

The FM signal is detected by a pulse averaging circuit, which includes monostable multivibrator (MVB) U4506A. The output from U4508-7 is applied to the "B" input of the MVB (pin 5). This MVB is triggered on the negative edge of the 9960 Hz input, and has an output pulse width of about 70 usec. The MVB is retriggerable if the next input pulse occurs within the 70 usec on-time.

The 9960 Hz pulse width is about 100 usec, and the unmodulated signal will produce evenly spaced 70 usec output pulses from the MVB (pin 6). However, the time between pulses will vary when the signal is modulated. Since the modulation is a constant 30 Hz reference frequency, the pulse spacing will vary at the 30 Hz rate. In other words, when the frequency is high, U4506A produces more pulses of constant width, and when it is lower the pulses are of the same width but further apart. The pulse width of the MVB is determined by the time constant developed by R135 and C4527.

The resulting pulses are averaged (integrated) by C4529, buffer amplifier U4505A, and low-pass filter U4504A. The resulting signal is a sinusoidal voltage that varies in amplitude at a 30 Hz rate. This signal is applied to 30 Hz band-pass filter U4503B. The filter output is applied to amplifier U4502, which produces the TTL level 30 Hz squarewave reference output at pin 7. This 30 Hz squarewave output is fed via J4512 pin 36 to the CNI digital module.

5 VOR Bearing Calculation

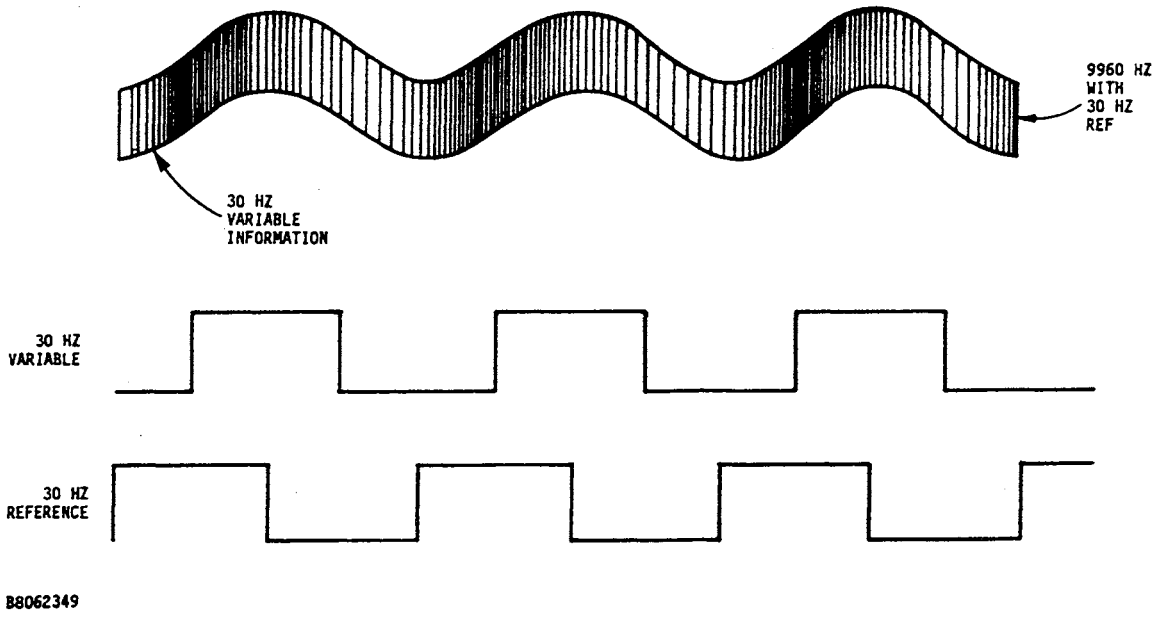
The CNI digital module switches the 30 Hz reference and the 30 Hz variable squarewave signals to the auxiliary module, where they are applied to programmable interval timers.

The NAV processor defines the VOR phase angle (radial) that the aircraft is on by a calculation using time differences. The processor measures the time difference between the 30 Hz reference and variable signals.

When the square wave signal goes positive a timer on the auxiliary module starts, defining T_o, the beginning of the 30 Hz reference period (P_1). When the 30 Hz variable square wave goes positive at T_1, the first time count stops, measuring the P_2 period.

The timer continues to time until it measures the period to the next positive going 30 Hz reference transition, T_2, the end of one complete 30 Hz reference cycle (P_1). (If the transmitted VOR signal 30 Hz reference frequency is not exactly 30 Hz, the processor compensates for the variance.)

Using the two measured time periods the processor divides P_2 by P_1, then multiplies the dividend times 360° to calculate the VOR angle.

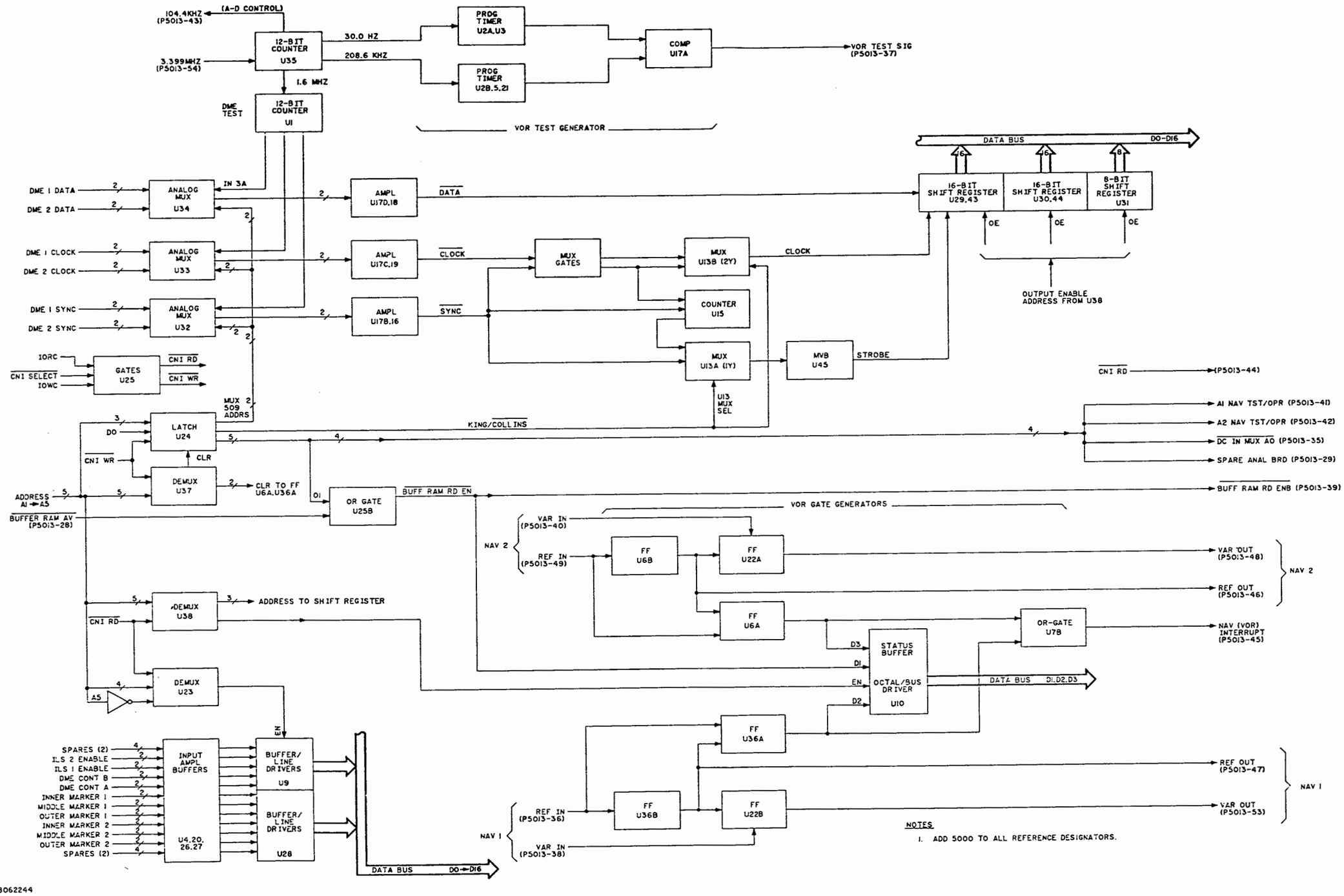


Typical VOR Composite Waveforms
Figure 87

(9) CNI Digital Modules 3605610-0501, -0502, and -0550

(a) General

This module processes the CNI digital signals from non-ARINC 429 equipment, and generates signals for incorporating into an ARINC 429 word. The inputs processed are listed in figure 89. Refer to the block diagram (figure 88) and to the module schematic diagram. The -0550 similar to the -0501, -0502 module except for HIRF lightning protection circuitry.



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CNI Digital Module, Simplified Block Diagram
Figure 88

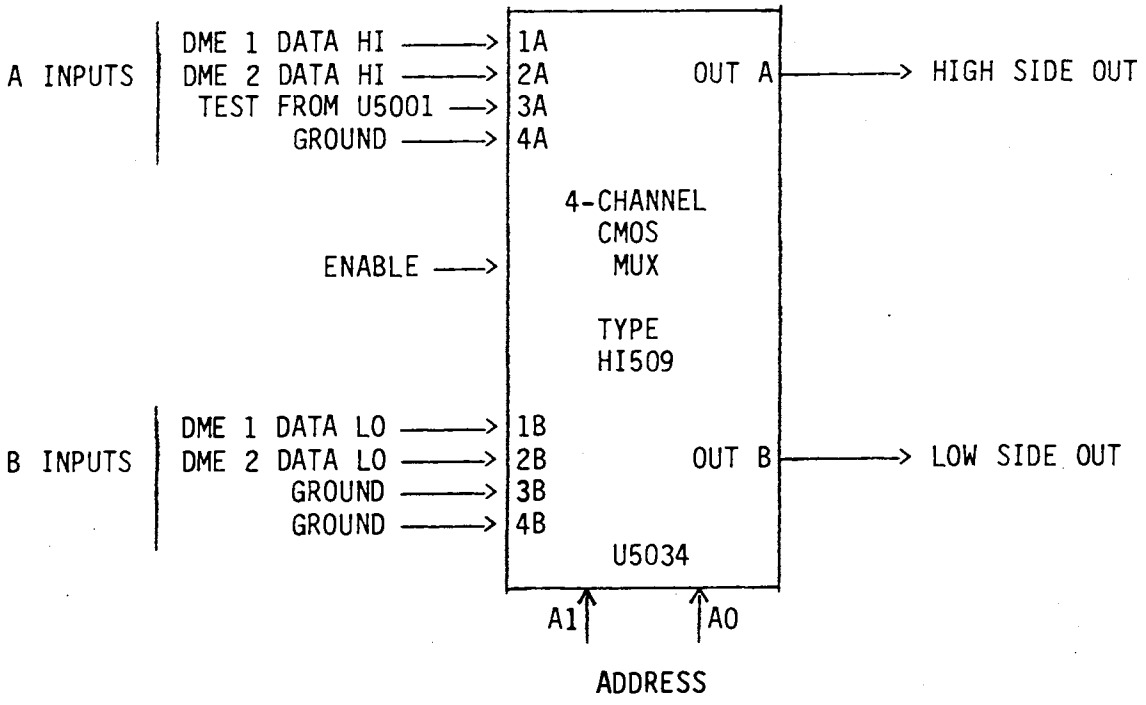
INPUTS	DESCRIPTION
DME 1 Data	Serial data to U5034
DME 2 data	Serial data to U5034
DME 1 Clock	Clock signals to U5033
DME 2 Clock	Clock signals to U5033
DME 1 Sync	DME sync to U5032
DME 2 Sync	DME sync to U5032
DME CONT A	Discrete input to U5004B
DME CONT B	Discrete input to U5004D
NAV 1	Discrete from CNI analog
NAV 2	Discrete from CNI analog
ILS 1 Enable	Discrete input to U5020C
Inner Marker 1	Discrete input to U5026A
Middle Marker 1	Discrete input to U5026B
Outer Marker 1	Discrete input to U5026D
ILS 2 Enable	Discrete input to U5020D
Inner Marker 2	Discrete input to U5026C
Middle Marker 2	Discrete input to U5027A
Outer Marker 2	Discrete input to U5027B

Inputs to CNI Digital Module
Figure 89

(b) Input Multiplexers

Several 4-channel CMOS analog multiplexers (type HI509) are contained on the module, and are used for selecting inputs to be processed. Refer to figure 89.

This chip has four "A" inputs and four "B" inputs, with a single "A" output and a single "B" output. When the chip is enabled by a logic high at pin 2, one of the "A" inputs will appear at the "A" output, and one of the "B" inputs will appear at the "B" output. A 2-bit address (A1, A0) determines which of the four inputs gets switched to the output.



Typical Analog Multiplexer Operation
Figure 90

(c) DME Circuits

The inputs from two DME's can be processed. Each DME supplies a DATA input, a CLOCK input, and a SYNC input to the module via connector J1B. The DME receivers in the aircraft supply two serial buses, for the left and right remote DME units. The two DME DATA inputs are applied to analog multiplexer U5034. Refer to figure 90 for typical multiplexer.

The DME selection is controlled by the microprocessor address signals and the CNI SELECT signal. The address signals (A1, A2, A3) are applied to an 8-bit addressable latch (U5024). Two of the latch outputs are applied to the three DME multiplexers (U5034, U5033, U5032) when the microprocessor wants to look at the DME DATA, CLOCK, and SYNC inputs. Each of the three multiplexers are addressed the same, and will select the inputs for either DME 1, DME 2, or test.

The two outputs (high side and low side) from the multiplexer are applied to a comparator, and the serial DATA is clocked into a serial-to-parallel shift register (U5029, U5043). The data is retrieved from the shift register on a polled basis at a 2.5 Hz clock rate as follows.

When power is applied, the test signal from counter U5001 is selected by the DME multiplexers (pin 6) and is routed into the DME circuit to clear the registers and verify circuit operation. The test signal is generated by the 12-bit counter U5001 from a 1.67 MHz input clock, and is in the King format (10101010.). The test signal is always selected by the address (A1, A0) between DME 1 and DME 2 selection to guarantee that no left-over data is processed, and to permit detecting a dead channel. Refer to figure 91.

ADDRESS		INPUTS SELECTED	DESCRIPTION
A1	A0		
0	0	1A & 1B	Selects DME 1 DATA for outputs.
0	1	2A & 2B	Selects DME 2 DATA for outputs.
1	0	3A & 3B	Selects clock for local DME test word.
1	1	4A & 4B	Both outputs go to ground (OFF condition).

DME Multiplexer Addresses
Figure 91

The outputs from the DME clock and sync multiplexers (U5033, U5032) are applied to circuits which are software controlled for the type DME installed in the system. The DME receiver circuits accept either the Collins DME format or the King DME format, which is determined by equipment strapping. The two formats are not totally compatible. When power is applied, the microprocessor reads the strap conditions and determines which type DME is connected. It then generates the necessary address to latch U5024, which supplies a King/Collins output to multiplexers U5013A and U5013B. This configures the hardware for selecting the King or Collins clock and strobe signals to the shift register.

(d) Clock Generator Circuits

The clock generator contains a 12-bit counter (U5035) and a 3.399 MHz input from the master processor module. The 3.399 MHz signal is divided by the counter to produce four additional frequencies for the CNI circuits. The clock frequencies obtained from U5035 are listed in figure 92.

FREQUENCY	U5035 PIN	APPLICATION
1.669 MHz	9	Drives DME test signal generator U5001.
208.686 kHz	3	Reference signal input to VOR test signal generator (divider U5003).
104.4 kHz	5	Drives A/D Buffer RAM control logic on analog CNI module (100 kHz).
30.000 Hz	15	Variable signal input to VOR test signal generator (divider U5021).

Clock Generator Frequencies
Figure 92

(e) Discrete Input Buffers

Several input buffer circuits allow discrete signals from the external equipment to be processed by the NC-104B. There are two types of buffers employed. The first type accepts "super flag" level signals which may be either sourcing +28 Vdc or an OPEN condition. The second type buffer input circuit can sense switched ground signals, which are either tied to an aircraft ground or are OPEN. The digital CNI module provides eight buffer inputs for each type, although they are not all employed.

All inputs employ a steering diode and a type LM139 operational amplifier, but the diode polarity and amplifier biasing is different for the two types inputs expected, and the inputs cannot be interchanged.

The 16 operational-amplifier outputs are applied to two octal buffer/line drivers, U5009 and U5028. When these two chips are enabled, they apply the discrete inputs to the data bus. The enable is obtained from the Y0 output of demultiplexer U5023, which is controlled by the address from the microprocessor. Refer to figure 93 for the discrete input read address (011000).

(f) Status Buffer U5010

This chip is an 8-bit bus driver which allows the microprocessor to view the different status bits as the CNI circuit collects data. To determine if data is ready to be read, this buffer is read by the microprocessor before any polling of the receiver circuits is performed. Although the chip may supply 8 bits to the data bus, only the D1, D2, and D3 outputs, for "Buffer RAM ready", "NAV 1 data ready", and "NAV 2 data ready" respectively, are employed.

This chip is enabled by an output from demultiplexer U5038, which is controlled by the address from the microprocessor and a CNI read signal (CNI RD). Refer to figure 93 for the status buffer read address (010110).

(g) VOR Gate Generators

There are two identical circuits provided, one for NAV 1 and one for NAV 2. Only the NAV 2 circuit is described.

The CNI analog module generates squarewave representations for the 30 Hz variable signal and for the reference signal. These two signals are used to produce two gate signals that control the programmable timers on the auxiliary module. The reference gate is the width of one cycle of the reference signal, and gives the processor circuits a reference count specifying the exact frequency of the 30 Hz signal being processed. The variable gate has a width equal to the reference gate at 0-degree phase shift and zero width at a 360-degree phase shift. The processor circuit determines the VOR bearing from the following formula, where the count occurs during the gate time.

$$\text{VOR bearing in degrees} = 360 \left(1 - \frac{\text{variable count}}{\text{reference count}}\right)$$

Using the reference count in the calculation eliminates any errors caused if the reference frequency is not exactly 30.0000 Hz.

The circuit also produces a "data ready" signal (from flip-flop U5006A) which appears as the D1 signal to the status buffer (U5010) and also generates the VOR Interrupt signal from U5007B, which is sent to the interrupt controller for the processor. The D1 output from the two VOR decoder circuits are or'd together in U5007B to produce a single "VOR Interrupt" signal. The processor determines which circuit originated the interrupt by reading the output from the status buffer.

To ensure that the data is not corrupted during writing to the buffer RAM, a request acknowledge protocol is employed between the processor and the controller hardware. When it is time for the processor to read the contents of the buffer RAM, it requests the sequencer to relinquish control of the address lines. When the controller reaches a point in the cycle where it is safe to mux the address lines, it does so, and sends a "ready", signal to the processor. The processor is then allowed to directly read data from the RAM and the controller will remain halted until the request signal is removed by the processor.

This circuit contains three identical D-type flip-flops, U5006A, U5006B, and U5022A. Assume that the Y3 output from demultiplexer U5037 has occurred and clears U5006A, which removes the NAV INTER signal. All three flip-flops are now in the reset condition and the Q output is a logic low.

When the first NAV 2 REF IN pulse occurs, it clocks U5006B to the set condition and the Q output goes high. This high output is the REF OUT signal and is also the "D" input to flip-flops U5022A and U5006A. When the NAV 2 VAR IN pulse occurs, U5022 will become set and produce a high VAR OUT signal.

When the next NAV 2 REF IN pulse occurs, U5006A becomes set and the high Q output is the NAV INTERRUPT signal. The low Q output from U5006A clears flip-flops U5006B and U5022A, and the circuit is now setup to receive the next VOR input to the processor.

(h) VOR Test signal Generator

This circuit generates a VOR NAV composite signal for testing and calibrating the VOR filter circuits. The crystal controlled 3.399 MHz clock is employed to digitally generate the signal, which eliminates any time or temperature drift errors that might enter into the calibration.

The 3.399 MHz clock is divided in U5035 to produce a 30.0 Hz output and a 208.6 kHz output as previously explained. The 30.0 Hz squarewave represents the "variable" component and is applied to U5021/U5005, which are programmable divide-by-N 4-bit counters. The 208.686 kHz output from U5035 represents the reference signal and is applied to divide-by-N counter U5003, which is programmed by the output from the 30 Hz counters. The two counter outputs are then summed together in summing amplifier U5017A to produce a 0-degree bearing composite VOR signal.

The test signal runs continuously and can be multiplexed into the detector circuits whenever required.

(i) Addresses

Most events and functions are timed or controlled by an address from the processor circuits, which result in read or write operations depending upon the IORC and IOWC signals. Figure 93 illustrates the various addresses for both the CNI analog and the CNI digital module operations previously described. Only addresses A1 through A5 in the 16-bit address are used on the CNI modules.

ADDRESS					READ FUNCTIONS		
A5	A4	A3	A2	A1	OPERATE	TEST	WRITE FUNCTIONS
0	0	0	0	0	#1 ADF SYNC X-Z	V ref	DC INPUT OPER/TEST select line
0	0	0	0	1	#2 ADF SYNC X-Z	GND	Buffer RAM read, Not used
0	0	0	1	0	#1 ADF SYNC Y-Z	V ref	not used
0	0	0	1	1	#2 ADF SYNC Y-Z	GND	#1 VOR $\overline{\text{OPERATE}}$/TEST
0	0	1	0	0	#1 LOC	V ref	#2 VOR $\overline{\text{OPERATE}}$/TEST
0	0	1	0	1	#2 LOC	GND	DME multiplexer address A0
0	0	1	1	0	#1 GS	V ref	DME multiplexer address A1
0	0	1	1	1	#2 GS	GND	$\overline{\text{Collins}}$/King DME format selection
0	1	0	0	0	RALT A (Collins)	V ref	not used
0	1	0	0	1	RALT B (Sperry)	GND	not used
0	1	0	1	0	RALT C (ARINC 552)	V ref	VOR 1 BEARING INTRPT reset (low)
0	1	0	1	1	RALT C offset test	GND	VOR 2 BEARING INTRPT reset (low)
0	1	1	0	0	#1 ADF sin	V ref	CLEAR BIT ADDRESSABLE CONTROL LATCH
0	1	1	0	1	#2 ADF sin	GND	not used
0	1	1	1	0	#1 ADF cos	V ref	not used
0	1	1	1	1	#2 ADF cos	GND	not used
1	0	0	0	0	DME word 1		
1	0	0	0	1	DME word 2		
1	0	0	1	0	DME word 3		
1	0	0	1	1	not used		
1	0	1	0	0	not used		
1	0	1	0	1	not used		
1	0	1	1	0	Status Buffer		not decoded for writing
1	0	1	1	1	not used		
1	1	0	0	0	Discrete Inputs		
1	1	0	0	1	not used		
1	1	0	1	0			
1	1	0	1	1			
1	1	1	0	0			
1	1	1	0	1			
1	1	1	1	0			
1	1	1	1	1	not used		

CNI Module Addresses
Figure 93

(j) DME Word Formats

Both the Collins DME words and the King DME words are processed by the CNI module as previously explained. Figure 94 illustrates the differences between the two formats.

FORMAT	DME WORD	DATA CONTENTS															
		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
COLLINS (ARINC)	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
	2	.08	.04	.02	.01	0	0	0	0	1	0	0	0	0	0	0	1
	3	SSM	SSM	200	100	80	40	20	10	8	4	2	1	0.8	0.4	0.2	0.1
KING	1	0.8	0.4	0.2	0.1	.08	.04	.02	.01	x	x	x	x	x	x	x	x
	2	x	x	x	x	x	x	200	100	80	40	20	10	8	4	2	1
	3	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

DME Word Format and Content
Figure 94

(10) Connector Board 200-08282-0000

The connector board, while providing all connections to the rear connector (J1A/B), also provides EMI filtering. The connector board replaces filter assembly 3606109-0501 and -0502.

The filtering circuit contains two steering diodes for isolation and an L-C filter. The left and right +28 Vdc buses are applied to steering (isolation) diodes on the board. the common output from the diodes is filtered by a conventional L-C filter and the dc voltage is applied to the power supply for developing the additional voltages required by the unit.